REMARKS/ARGUMENT

Claims 6, 7, 14 and 15 have been amended better to define the claimed invention and overcome the 35 U.S.C. 112, second paragraph, rejection.

1) Claims 1, 3, 7, 9, 11, 15-20 and 22 stand rejected under 35 U.S.C. 102(b) as being anticipated by Tremblay et al. [6,125,439]. Applicants respectfully traverse this rejection, as set forth below.

In order that the rejection of Claims 1, 3, 7, 9, 11, 15-20 and 22 be sustainable, it is fundamental that "each and every element as set forth in the claim be found, either expressly or inherently described, in a single prior art reference." *Verdegall Bros. v. Union Oil Co. of California*, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987). See also, *Richardson v. Suzuki Motor Co.*, 9 USPQ2d 1913, 1920 (Fed. Cir. 1989), where the court states, "The identical invention must be shown in as complete detail as is contained in the ... claim".

Furthermore, "all words in a claim must be considered in judging the patentability of that claim against the prior art." *In re Wilson*, 424 F.2d 1382, 1385, 165 USPQ 494, 496 (CCPA 1970).

Independent Claim 1, requires and positively recites, a processor, comprising: "a processing core that generates memory addresses to access a main memory and on which a plurality of methods operate, each method using its own set of local variables", "and a cache subsystem comprising a multi-way set associative cache **and a data memory that**

holds a contiguous block of memory defined by an address stored in a register, wherein local variables are stored in said data memory".

Independent Claim 9, requires and positively recites, a cache subsystem, comprising: "a multi-way set associative cache" and "a data memory that holds **a contiguous block of memory defined by an address stored in a register**, wherein **local variables are stored in said data memory**".

Independent Claim 17, requires and positively recites, a cache subsystem, comprising: "a multi-way set associative cache" and "a means for **holding a contiguous block of memory defined by an address stored in a register, wherein local variables are stored in said data memory**".

Independent Claim 20, requires and positively recites, a method, comprising: "programming a register to define **a contiguous block of memory in a cache subsystem**" and "storing **local variables** associated with executing methods **in the contiguous block of memory**.

In contrast, there is no teaching in Tremblay that teaches or suggests, **a data memory that holds a contiguous block of memory defined by an address stored in a register**. Should the Examiner disagree, Applicants respectfully request that the Examiner point out such teaching.

Further, Tremblay specifically states that its local variables are stored in the stack – NOT a data memory. More particularly, Tremblay states:

> The **local variable area on stack** 400 (FIG. 4A) for current method 410 represents temporary variable storage space which is allocated and remain effective during invocation of method 410 (col. 9, lines 48-51).
>
> When a method is executing on hardware processor 100, **the local variables typically reside in stack cache 155** and are addressed as offset from pointer VARS (FIGS. 1 and 4A), which points to the position of the local variable zero. Instructions are provided to load the values of local variables onto operand stack 423 and store values from operand stack into local variables area 421 (col. 9, lines 55-61).

In light of the above, Tremblay fails to teach or suggest, "... a cache subsystem comprising a multi-way set associative cache **and a data memory that holds a contiguous block of memory defined by an address stored in a register, wherein local variables are stored in said data memory**", as required by Claim 1, OR "a data memory that holds **a contiguous block of memory defined by an address stored in a register**, wherein **local variables are stored in said data memory**", as required by Claim 9, OR "a means for **holding a contiguous block of memory defined by an address stored in a register, wherein local variables are stored in said data memory**", as required by Claim 17, OR "programming a register to define **a contiguous block of memory in a cache subsystem**" and "storing **local variables** associated with executing methods **in the contiguous block of memory**", as required by Claim 20.

Accordingly, the 35 U.S.C. 102(b) rejection of Claims 1, 9, 17 and 20 is improper and must be withdrawn since all of the elements of Claims 1, 9, 17 or 20, respectively, cannot be found in the Tremblay reference.

Claims 3, 7, 11, 15, 16, 18, 19 and 22 stand allowable as depending (directly or indirectly) from allowable independent claims and by including further limitations not taught or suggested by the reference of record.

Claim 3 further defines the processor of claim 1 wherein when a new method is called, the local variables associated with the called method use data memory space previously used by local variables associated with completed methods without generating a miss. Claim 3 depends from Claim 1 and is therefore allowable for the same reasons set forth above for the allowance of Claim 1.

Claim 7 further defines the processor of claim 1 wherein, if said data memory does not have sufficient capacity to store the local variables, then at least some local variables are stored in the 2-way set associative cache. Claim 7 depends from Claim 1 and is therefore allowable for the same reasons set forth above for the allowance of Claim 1.

Claim 11 further defines the cache subsystem of claim 9 wherein when a new method is called, the local variables associated with the called method use data memory space previously used by local variables associated with completed methods without generating a miss. Claim 11 depends from Claim 1 and is therefore allowable for the same reasons set forth above for the allowance of Claim 1.

Claim 15 further defines the cache subsystem of claim 9 wherein, if said data memory does not have sufficient capacity to store the local variables, then at least some local variables are stored in the multi-way set associative cache. Claim 15 depends from Claim 9 and is therefore allowable for the same reasons set forth above for the allowance of Claim 9.

Claim 16 further defines the cache subsystem of claim 15 wherein said local variables comprise local variables used in a stack-based instruction set. Claim 16

depends from Claim 15 and is therefore allowable for the same reasons set forth above for the allowance of Claim 15.

Claim 18 further defines the cache subsystem of claim 17 further including a means for locking said local variables in said cache subsystem. Claim 18 depends from Claim 17 and is therefore allowable for the same reasons set forth above for the allowance of Claim 17.

Claim 19 further defines the cache subsystem of claim 17 further including a means for preventing said local variables from being written to external memory upon completion of a method that uses said local variables. Claim 19 depends from Claim 17 and is therefore allowable for the same reasons set forth above for the allowance of Claim 17.

Claim 22 further defines the method of claim 20 further comprising invoking a new method and writing local variables associated with the new method to cache memory space previously used by local variables associated with completed methods without generating a miss. Claim 22 depends from Claim 20 and is therefore allowable for the same reasons set forth above for the allowance of Claim 20.

2) Claims 6 and 14 stand rejected under 35 U.S.C. 103(a) as being unpatentable over Tremblay et al. Applicants respectfully traverse this rejection, as set forth below.

In proceedings before the Patent and Trademark Office, "the Examiner bears the burden of establishing a prima facie case of obviousness based upon the prior art". *In re Fritch*, 23 USPQ2d 1780, 1783 (Fed. Cir. 1992) (citing *In re Piasecki*, 745 F.2d 1468,

1471-72, 223 USPQ 785, 787-88 (Fed. Cir. 1984). "The Examiner can satisfy this burden **only by showing some objective teaching in the prior art or that knowledge generally available to one of ordinary skill in the art would lead that individual to combine the relevant teachings of the references**", *In re Fritch*, 23 USPQ2d 1780, 1783 (Fed. Cir. 1992)(citing *In re Fine*, 837 F.2d 1071, 1074, 5 USPQ2d 1596, 1598 (Fed. Cir. 1988)(citing *In re Lalu*, 747 F.2d 703, 705, 223 USPQ 1257, 1258 (Fed. Cir. 1988)).

Similarly, "obviousness cannot be established by combining the teachings of the prior art to produce the claimed invention, **absent some teaching or suggestion supporting the combination. Under section 103, teachings of references can be combined ONLY if there is some suggestion or incentive to do so.**" *ACS Hosp. Systems, Inc. v. Montefiore Hosp.*, 732 F.2d 1572, 1577, 221 USPQ 929, 933 (Fed. Cir. 1984).

Similarly, although couched in terms of combining teachings found in the prior art, the same inquiry must be carried out in the context of a purported obvious "modification" of the prior art. **The mere fact that the prior art may be modified in the manner suggested by the Examiner does not make the modification obvious unless the prior art suggested the desirability of the modification**. *In re Gordon*, 733 F.2d at 902, 221 USPQ at 1127. Moreover, **it is impermissible to use the claimed invention as an instruction manual or "template" to piece together the teachings of the prior art so that the claimed invention is rendered obvious**. *In re Gorman*, 933 F.2d 982, 987, 18 USPQ2d 1885, 1888 (Fed.Cir.1991). See also *Interconnect Planning Corp. v. Feil*, 774 F.2d 1132, 1138, 227 USPQ 543, 547 (Fed.Cir.1985).

Claim 6 further defines the processor of claim 1 wherein the data memory containing the local variables has a higher priority during hit/miss determinations.

Claim 14 further defines the cache subsystem of claim 9 wherein the data memory containing the local variables has a higher priority during hit/miss determinations.

As stated above, Tremblay fails to teach or suggest, "... a cache subsystem comprising a multi-way set associative cache **and a data memory that holds a contiguous block of memory defined by an address stored in a register, wherein local variables are stored in said data memory**", as required by Claim 1, OR "a data memory that holds **a contiguous block of memory defined by an address stored in a register**, wherein **local variables are stored in said data memory**", as required by Claim 9. For this reason alone, Claims 6 and 14 are allowable over Tremblay.

Further, even if Tremblay had taught all of the above high-lighted elements in Claim 1 and 9, Claims 6 and 14 are patentable over Tremblay.

Applicants traverse the Examiner's conclusion that, since Tremblay discloses that a request from data cache to external memory always has a higher priority than instruction cache request to external memory as a result of arbitration logic between internal and external components, it would have been obvious to one ordinarily skilled in the art at the time of Applicants' invention that since hit/miss determination might result in access to external memory, higher priority should be given to such data memory during that process, in order to allow the external memory access arbitration logic of Tremblay et al. to grant a higher priority to data cache requests to external memory. (Office Action, page 6, lines 1-10).

Tremblay states:

> I/O bus and memory interface unit 110 generates read and write requests to external memory. Specifically, interface unit 110 provides an interface for

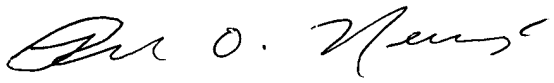
> instruction cache and data cache controllers 121 and 161 to the external memory. Interface unit 110 includes arbitration logic for internal requests from instruction cache controller 121 and data cache controller 161 to access external memory and in response to a request initiates either a read or a write request on the memory bus to the external memory. **A request from data cache controller 161 is always treated as higher priority relative to a request from instruction cache controller 121** (col. 11, lines 48-58).

The above teaching has nothing to do with determining priority between internal and external components, as suggested by the Examiner. It has to do with determining priority between two internal components – data cache controller 161 and instruction cache controller 121. As such, the teaching would not have been relevant to one ordinarily skilled in the art at the time of Applicants' invention in leading him to conclude that "data memory containing local variables has a higher priority during hit/miss determinations", as required by Claims 6 and 14. The Examiner's determination is supposition not supported by fact and is nothing more than hind sight reconstruction. As set forth by case law, **it is impermissible to use the claimed invention as an instruction manual or "template" to piece together the teachings of the prior art so that the claimed invention is rendered obvious**. As such, Claims 6 and 14 are allowable over Tremblay under 35 USC 103(a).

Applicants' appreciate the Examiner's indication that Claims 2, 4, 5, 8, 10, 12, 13, 21 and 23 would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims, but Applicants submit that these claims are allowable in their present form.

Claims 1-23 stand allowable. Applicants respectfully request withdrawal of the rejections and allowance of the application at the earliest possible date.

Respectfully submitted,



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